In The Claims

Please amend independent claim 15 as follows:

15. (Twice Amended) A thin film transistor structure, comprising:

an insulating substrate;

a polysilicon layer over the substrate;

a gate structure over the polysilicon layer, wherein the gate structure includes a gate layer, a gate dielectric layer between the gate layer and the polysilicon layer and a spacer on each side of the gate layer, wherein the spacer with respect to a surface of the gate dielectric layer and a surface of the polysilicon layer forms a contrast surface; and

a selective conductive layer over the gate layer and the polysilicon layer adjacent to the spacers based on the contrast surface, wherein the selective conductive layer adjacent to the spacers serves as a source/drain region without additionally implanting process on the source/drain region.

REMARKS

Present Status of the Application

The Office Action rejected presently-pending claims 15-20. Specifically, the Office Action rejected claims 15 and 16 under 35 U.S.C. 103, as being unpatentable over Applicant's Prior Art (APA) in view of Wu (U. S. Patent No. 5,977,561) and Cho et al. (U. S. Patent No. 5,578,838). In addition, the Office Action rejected claim 17 under 35 U.S.C. 103, as being unpatentable over